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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,700	07/31/2003	In-Ku Kang	8750-045	3617

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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,700	KANG ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 17 is objected to because of the following reasons.

In claim 17, line 10, "...a insulating tape..." is misspelled. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 7-12, 14, 16-19, 23-25 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of U.S. Patent No. 6,552,426 to Ishio et al. (herin after Ishio).

Regarding to claim 1, Background of the Invention discloses a multi-chip module comprising a substrate 21 having a plurality of interconnections 21a, 21b formed on a top surface thereof; a lowest chip 23 and at least one top chip 27 sequentially stacked on the top surface, the lowest chip and the top chip each having pads 23a, 27a formed thereon;

an insulator 29 interposed between the chips 23, 27, the insulator 29 exposing the pads 23a; and a first group of bonding wires 31connecting the pads 23a of the lowest chip 23 with a first group of interconnections 21a on the substrate 21 (fig. 2).

However, Background of the Invention does not disclose the top chip having an insulating tape attached to a backside thereof. Ishio teaches the top chip having an insulating tape attached thereof as set forth in column 5, lines 33-67, column 6, lines 1-59, figs. 1, 9.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top chip having an insulating tape attached to a backside thereof, as taught by Ishio in order to provide a quality and reliable high-density package semiconductor device without problems related to the manufacturing process (col. 2,lines 55-60).

Regarding to claims 2 and 18, Background of the Invention discloses the multi-chip module further comprising a second group of bonding wires 33 connecting the pads 27a of the top chip 27 with a second group of interconnections 21b on the substrate 21.

Regarding to claims 3 and 12, Background of the Invention discloses the multi-chip module wherein all the chips have substantially the same dimension and fully cover each other (fig. 2).

Regarding to claim 5, 14, and 19, Background of the Invention discloses the multi-chip module further comprises an adhesive 25 interposed between the lowest chip 23 and the substrate 21 (fig. 2).

Regarding to claims 7, 16, and 23, Background of the Invention discloses the claimed invention except for the multi-chip module further comprises an epoxy molding compound that encapsulates the stacked chips and the bonding wires. Ishio teaches the multi-chip module further comprises an epoxy molding compound 10 that encapsulates the stacked chips and the bonding wires (col. 5, lines 55-59, and figs 1, 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an epoxy molding compound that encapsulates the stacked chips and the bonding wires, as taught by Ishio in order to cover at least the wires and to prevent from being damaged (col. 5, lines 56-58).

Regarding to claims 8, Background of the Invention discloses the multi-chip module wherein the lowest chip 23 and the top chip 27 each have peripheral pads 23a, 27a formed on a top surface thereof (fig. 2).

Regarding to claim 9, Background of the Invention discloses the multi-chip module wherein the insulator 29 has a smaller width than the chips 23, 27 to expose the pads 23a, 27a (fig. 2).

Regarding to claim 10, Background of the Invention discloses a multi-chip module comprising a bottom chip 23 and a top chip 27 sequentially stacked on the top surface, and the bottom chip 23 and the top chip 27 each having peripheral pads 23a, 27a on a top surface thereof; an insulator 29 interposed between the bottom chip 23 and the top chip 27, the insulator having a smaller width than the chips to expose the pads 23a of the bottom chip 23 (fig. 2); a first group of bonding wires 31 connecting the pads 23a of the bottom chip 23 with the first group of interconnections 21a; and a second group of bonding wires 33 connecting the pads 27a of the top chip 27 with the second group of interconnections 21b (fig. 2).

Background of the Invention does not disclose the top chip having an insulating tape attached to its backside. Ishio teaches the top chip having an insulating tape attached to it as set forth in column 5, lines 33-67, column 6, lines 1-59, figs. 1, 9.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top chip having an insulating tape attached to its backside, as taught by Ishio in order to provide a quality and reliable high-density package semiconductor device without problems related to the manufacturing process (col. 2,lines 55-60).

Regarding to claim 11, Background of the Invention discloses the multi-chip module wherein the substrate is a lead frame or a printed circuit board (page 2, lines 5-6).

Regarding to claim 17, Background of the Invention discloses a method of fabricating a multi-chip module, the method comprising: preparing a substrate 21 having first and second groups of interconnections 21a, 21b formed on a top surface thereof; mounting a bottom chip 23 on the top surface, the bottom chip 23 having pads 23a formed thereon; forming a first group of bonding wires 31 that connect the pads 23a of the bottom chip 23 to the first group of interconnections 21a; attaching an insulator 29 on an upper surface of the bottom chip 23, the insulator 29 being surrounded by the pads 23a of the bottom chip 23; and mounting a top chip 27 on the insulator 29, the top chip having pads 27a formed thereon (fig. 2).

However, Background of the Invention does not disclose the top chip including an insulating tape attached to a backside thereof. Ishio teaches the top chip including an insulating tape attached bthereof as set forth in column 5, lines 33-67, column 6, lines 1-59, figs. 1, 9.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top chip including an insulating tape attached to a backside thereof, as taught by Ishio in order to provide a quality and reliable high-density package semiconductor device without problems related to the manufacturing process (col. 2,lines 55-60).

Regarding to claim 24, Background of the Invention discloses the method wherein the pads 23a, 27a are formed on edges of the top surfaces of the chips (fig. 2).

Regarding to claim 25, Background of the Invention discloses the method wherein the insulator 29 is attached on a central region of the bottom chip 23, thereby having a width smaller than the bottom chip 23 and the top chip 27 (fig. 2).

Claims 4 and 13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of Koopmans (US Patent No. 6,706,557).

Background of the Invention discloses the claimed invention except for the multi-chip module wherein the top chip has a greater planar area than the lowest chip located thereunder. Koopmans teaches the top chip has a greater planar area than the lowest chip located thereunder (column 8, lines 51-61, and fig. 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top chip has a greater planar area than the lowest chip located thereunder, as taught by Koopmans in order to obtain higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits. One way to achieve greater integrated circuit density is by attaching two or more semiconductor dice or chips in a single semiconductor assembly (col. 2, lines 10-17).

Claims 6, 15, 20, and 22 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of Lin (US Patent No. 6,333,562).

Regarding to claims 6 and 15, Background of the Invention discloses the claimed invention except for the multi-chip module further comprises bumps formed on the pads of the chips, the bonding wires being in contact with the bumps. Lin teaches the multi-chip module further comprises bumps 350 formed on the pads 310a of the chips 310, the bonding wires 360 being in contact with the bumps 350 (col. 4, lines 10-65, and fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the multi-chip module further comprises bumps formed on the pads of the chips, the bonding wires being in contact with the bumps, as taught by Lin in order to provide a multi-chip module comprising two chips disposed on means for supporting chips in a stacking arrangement and respectively wire bonded to the supporting means wherein the multi-chip module is characterized by having a plurality of electrically conductive bumps interposed between the stacked chips to serve as a spacer therebetween thereby keeping the upper chip from damaging the bonding wires of lower chip (col. 2, lines 35-44).

Regarding to claim 20, Background of the Invention discloses the claimed invention except for the method further comprises forming bumps on the pads of the bottom chip before forming the first group of bonding wires, the first group of bonding

wires being connected to the bumps on the pads of the bottom chip. Lin teaches forming bumps 350 on the pads 310a of the bottom chip 310, the bonding wires 360 being in contact with the bumps 350 (col. 4, lines 10-65, and fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form bumps on the pads of the bottom chip before forming the first group of bonding wires, the first group of bonding wires being connected to the bumps on the pads of the bottom chip, as taught by Lin in order to provide a multi-chip module comprising two chips disposed on means for supporting chips in a stacking arrangement and respectively wire bonded to the supporting means wherein the multi-chip module is characterized by having a plurality of electrically conductive bumps interposed between the stacked chips to serve as a spacer therebetween thereby keeping the upper chip from damaging the bonding wires of lower chip (col. 2, lines 35-44).

Regarding to claim 22, Background of the Invention discloses the claimed invention except for the method further comprises forming bumps on the pads of the top chip before forming the second group of bonding wires, the second group of bonding wires being connected to the bumps on the pads of the top chip. Lin teaches forming bumps on the pads of the top chip before forming the second group of bonding wires, the second group of bonding wires being connected to the bumps (col. 4, lines 10-65, and fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form bumps on the pads of the top chip before forming the second group of bonding wires, the second group of bonding wires being connected to the bumps on the pads of the top chip, as taught by Lin in order to provide a multi-chip module comprising two chips disposed on means for supporting chips in a stacking arrangement and respectively wire bonded to the supporting means wherein the multi-chip module is characterized by having a plurality of electrically conductive bumps interposed between the stacked chips to serve as a spacer therebetween thereby keeping the upper chip from damaging the bonding wires of lower chip (col. 2, lines 35-44).

Claim 21 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of US Patent Application Publication 2003/0038374 to Shim et al. (herein after Shim).

Background of the Invention discloses the claimed invention except for the method wherein the first group of bonding wires are formed using a bump reverse bonding technique. Shim teaches the first group of bonding wires are formed using a bump reverse bonding techniques (page 2, paragraph [0028]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first group of bonding wires using a bump reverse bonding technique, as taught by Shim in order to reduce the total thickness of the package (col. 2, paragraph [0028]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MHT
08/20/04

Mai-Huong Tran
Examiner
Art Unit 2818